A Signal Processing Board for Gamma-Ray Tracking Detectors

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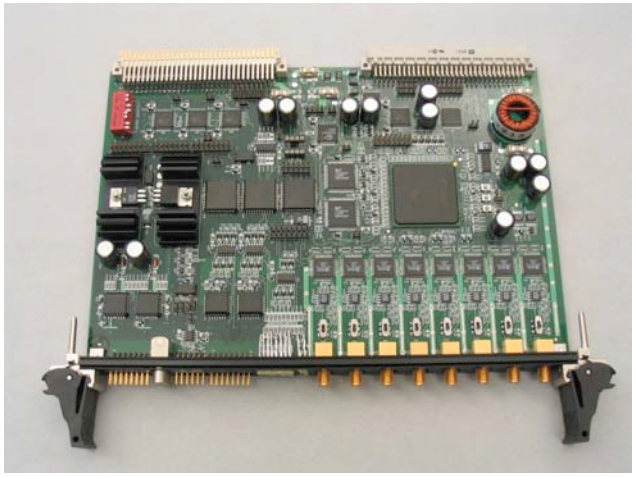
Digital electronics are an integral part of gamma-ray tracking detectors, such as GRETINA, as one is required to sample the preamplifier signal from each segment during charge collection to identify the location and charge deposited by gamma rays scattering through the HPGe Crystal. To accomplish this task, we have developed a prototype 8-channel, VME-based, signal processing board (Fig. 1) which continuously samples at a rate of 100 MHz with a 12-bit dispersion. The board was also designed to meet the more general requirements for a signal processor board as specified by the Argonne workshop on digital electronics (2001) for low-energy nuclear physics experiments.

This board is differs from most commercial digitizers in that it emulates, in a single large FPGA, much of the functionality found in analog systems for Ge detectors. Segment energies are calculated on the board from the trace obtained from the detectors preamplifier using a digitally implemented trapezoidal shaper [1]. This means that only the part of the trace which contains information relevant to signal decomposition needs to be extracted, rather than the significantly longer trace required to recover proper energy resolution. This dramatically reduces the data which is transfered on the VME backplane and allows the board to operate at standard Ge rates (several kHz). Constant fraction times, pile-up detection and windowing algorithms (which are responsible for extracting the relevant part of the trace) are also implemented on the board.

Each channel of the board can be independently triggered and three triggering modes are provided; internal, external and validate modes. In internal mode a channel of the signal processing board is triggered by an internal, digitally implemented, leading edge discriminator. Each discriminator is accessible as an ECL logic pulse at the front-panel. In external mode, the channel is triggered by an externally provided ECL logic pulse input on the boards front panel. In validate mode, the board is triggered if the leading edge discriminator fires followed by an externally provided ECL logic signal which validates the event.

Associated with each event produced by a valid trigger is a 48 bit timestamp, incremented at the digitization rate, which allows for event building between digitizer boards. Each board can be configured to operate from an external clock to synchronize these timestamps. Each board contains a 1 Mb output FIFO to store events before they are read out. These events contain an event header (which includes the energy, leading edge and constant fraction time, segment and board ID) and a section of the trace from the triggered channel. Mechanisms to support both polled and interrupt driven acquisition systems are provided. Board configuration is also done over the VME backplane where the integration time for the energy, the position of the trace windows, discriminator levels and constant fraction discriminator parameters can be set. Provision was also made to reprogram the FPGA over the VME backplane.

FIG. 1: Photograph of the Gretina prototype digitizer module.



Several prototype signal digitizers were constructed and successfully used in source tests with clover detectors and in in-beam tests with the Greta prototype–2, 36-segment detector. Recently, the production of 15 boards to fully instrument the 3-crystal Gretina module prototype has been completed and will be used to perform end-to-end detector testing.

[1] V. Jordanov, Nucl. Instr. and Meth. A **345**, 337 (1994).